REMARKS

In view of the foregoing amendments and the following remarks, reconsideration and allowance are requested.

Claims 21-23, 25, 42-64 and 68-70 are pending, with claims 21, 47 and 56 being independent. Claims 1-20, 24, 26-41 and 65-67 have been canceled, and claims 21, 47 and 56 have been amended. No new matter has been presented.

Claim Rejection under 35 U.S.C. § 112

Claims 21-23, 25, 42-64 and 68-70 stand rejected under 35 U.S.C. 112, second paragraph, as a result of the recitation in independent claims 21, 47 and 56 of "to remove a catalytic element," for which there is alleged to be insufficient antecedent basis. Without conceding the propriety of the rejection, this feature has been removed from claims 21, 47 and 56 in the current claim amendments. Accordingly, this rejection should be withdrawn.

Claim Rejection under 35 U.S.C. § 103

Claims 21, 42, 43, 47, 51 and 52 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki (JP 08-288515A) (which corresponds to U.S. Patent No. 5,759,879) in view of Ueda (U.S. Patent No. 5,395,804). With respect to claims 21, 47 and 56, applicants request reconsideration and withdrawal of the rejection at least because neither Iwasaki, Ueda, nor any proper combination of the two describes or suggests that "lattices are continuously connected to each other at substantially all of a grain boundary of said semiconductor film between different crystals," as recited in claims 21, 47 and 56.

Iwasaki describes a method for forming a polycrystalline silicon film for a thin film transistor (TFT) where "a channel region including crystals having uniform orientation can be obtained **without having grain boundaries** in a direction of the current path," for which "**there are no defects** which will cause a current barrier or a leakage current" (Iwasaki: Abstract, col. 15:46-53, emphasis added). FIGS. 3F and 3G (reproduced below) show views of a process of fabricating a TFT, and FIG. 4B (reproduced below) shows a view where a think polycrystalline silicon film is used for forming a side wall.

FIG. 3F

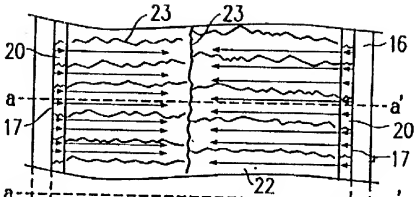


FIG. 3G

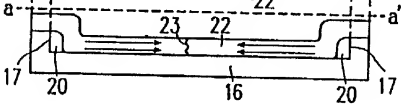
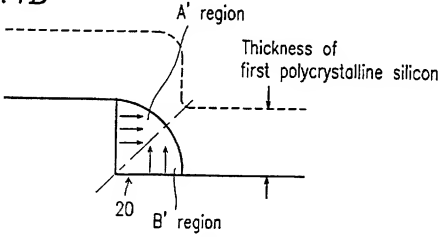


FIG. 4B



Iwasaki describes that, as shown in FIGS. 3F and 3G, crystals in the polycrystalline silicon film 22 grow to have a uniform orientation in a direction perpendicular to the side of the step 17 and "**no grain boundaries substantially exist** in the direction of the current path," (Iwasaki: cols. 10:67-67, 11:1-4) (emphasis added). With respect to FIGS. 5A, 5B, 6A and 6B, Iwasaki discloses that "no grain boundaries substantially exist across the current path of each TFT" (Iwasaki: cols. 13:16-18, 14:6-8). With respect to FIGS. 4A and 4B, Iwasaki describes

that the side wall 20 includes an A region and a B region having crystal orientations different from each other, where the crystal orientation of the A region is in a lateral direction, and that of the B region is in a vertical direction (Iwasaki: col. 11:30-60).

Iwasaki does not describe or suggest that "lattices are continuously connected to each other at substantially all of a grain boundary of said semiconductor film between different crystals," as recited in claims 21, 47 and 56, because Iwasaki is silent on describing how the lattices are connected to each other at substantially all of a grain boundary, and because Iwasaki teaches how to avoid forming grain boundaries in the semiconductor film across the current path of the TFT. The Office Action asserts that Iwasaki inherently describes that there is a grain boundary between different crystals of the polycrystalline silicon film 22. However, Iwasaki teaches fabrication techniques in the semiconductor film so that "**there are no defects** which will cause a current barrier or a leakage current" (Iwasaki: col. 15:46-53, emphasis added). Moreover, **Iwasaki teaches fabrication methods that prevent the formation of grain boundaries in the semiconductor film** of the TFT, and none of the embodiments in Iwasaki describe or suggest how the lattices are connected to each other at substantially all of the grain boundary in the semiconductor film between different crystals.

Ueda, which is cited as describing "atoms constituting the different crystals at the grain boundary correspond to each other respectively or have dangling bonds neutralized by hydrogen and halogen elements," fails to remedy the deficiencies of Iwasaki in describing or suggesting the features recited above for claims 21, 47 and 56. For at least these reasons, the rejection of independent claims 21, 47 and 56, and their respective dependent claims, should be withdrawn.

Claims 22 and 48, which depend from claims 21 and 47, respectively, have been rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki and Ueda, and further in view of Erhart (U.S. Patent No. 5,572,211). Erhart, which is cited as describing capacitors and thin film transistors in an active matrix display in a personal computer, does not remedy the failure of Iwasaki and Ueda to describe or suggest the features of claims 21 and 47 discussed above. For at least these reasons, the rejection of claims 22 and 48 should be withdrawn.

Claims 23, 25, 46, 49, 50 and 55, which depend from claims 21 and 47, have been rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki and Ueda, and further in view of den Boer (U.S. Patent No. 5,539,219). Den Boer, which is cited as describing an active

matrix liquid crystal display device with TFTs, pixel electrodes and a common electrode, does not remedy the failure of Iwasaki and Ueda to describe or suggest the features of claims 21 and 47 discussed above. For at least these reasons, the rejection of claims 23, 25, 46, 49, 50 and 55 should be withdrawn.

Claims 44, 45, 53 and 54, which depend from claims 21 and 47, have been rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki and Ueda, and further in view of Kobayashi (U.S. Patent No. 3,925,803). Kobayashi, which is cited as describing a field effect transistor that has a polycrystalline structure on its channel region, does not remedy the failure of Iwasaki and Ueda to describe or suggest the features of claims 21 and 47 discussed above. For at least these reasons, the rejection of claims 44, 45, 53 and 54 should be withdrawn.

Claims 56, 60 and 61 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki in view of Inoue (U.S. Patent No. 6,153,893) and Ueda. Claim 57, which depends from claim 56, has been rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki, Inoue and Ueda, in view of Erhart; claims 58, 59 and 64, which depend from claim 56, have been rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki, Inoue and Ueda, in view of den Boer; Claims 62 and 63, which depend from claim 56, have been rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki, Inoue and Ueda, in view of Kobayashi. Inoue, which is cited as describing a thin film transistor with a lightly doped drain (LDD) structure, does not remedy the failure of Iwasaki, Inoue and Ueda to describe or suggest the features of claim 56 discussed above. As noted above, Erhart, den Boer and Kobayashi also fail to do so. For at least these reasons, the rejections of claims 56-64 should be withdrawn.

Claims 68-70, which depend from claims 21, 47 and 56, respectively, have been rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki, Ueda, and further in view of Tran (U.S. Patent No. 5,534,445). Tran, which is cited as describing a polysilicon-based TFT that has a silicon wafer for providing a substrate underneath an insulating layer from which a semiconductor film is grown, does not remedy the failure of Iwasaki and Ueda to describe or suggest the features of claims 21, 47 and 56 discussed above. For at least these reasons, the rejection of claims 68-70 should be withdrawn.

All claims are in condition for allowance.

Conclusion

It is believed that all of the pending issues have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this reply should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this reply, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Fees in the amount of $490 for a two-month extension of time and $810 for a Request for Continued Examination (RCE) are being paid concurrently herewith on the Electronic Filing System (EFS) by way of Deposit Account authorization. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: April 14, 2011

/Dwight U. Thompson/
Dwight U. Thompson
Reg. No. 53,688

Customer Number 26171
Fish & Richardson P.C.
Telephone: (202) 783-5070
Facsimile: (877) 769-7945